What is claimed is:

1. An information processor, comprising:

a CPU;

an input/output device that is provided with an input device for applying data or commands as input to said CPU and an output device for supplying as output commands or the results of data processing that are issued from said CPU;

two chip sets that are each provided with a serial controller, said chip sets operating as a working system that normally operates or a reserve standby system, said chip sets being an I/O interface that is interposed between said CPU and said input/output device;

a selector for switching the connection routes of said serial controllers and said input/output device when a fault occurs in one of said two chip sets; and

a service processor for controlling said selector to cause the output data of said serial controller of said working system to be supplied to said output device and data from said input device to be supplied to each of said two serial controllers when no fault has occurred in said chip sets, and upon receiving notification of the occurrence of a fault from either one of said chip sets, to cause

only output data of the serial controller that is provided in the chip set that is operating normally to be supplied as output to said output device and to cause data from said input device to be supplied only to the serial controller that is provided in the chip set that is operating normally.

2. The information processor according to claim 1, wherein each of said serial controllers comprises:

a command buffer for temporarily holding commands that are transmitted from said CPU;

an input buffer for temporarily holding data that are received as input using said input device;

a serial data input/output unit for transmitting data between said CPU and said input/output device; and

a serial synchronizing unit for synchronizing the operations of the two serial controllers.

3. The information processor according to claim 2, wherein:

when a fault has not occurred in said chip sets, and moreover, when a command from said CPU is

stored in said command buffer, said serial synchronizing unit of said working system requests said serial synchronizing unit of said standby system for permission to execute said command; and

said serial synchronizing unit of said standby system, upon receiving said request for permission to execute, and moreover, when said command is stored in said command buffer, both sends permission to execute said command to said serial synchronizing unit of said working system and causes said serial data input/output unit to execute processing of said command.

4. The information processor according to claim 2, wherein:

when a fault has not occurred in said chip sets and when data from said input device have been stored in said input buffer, said serial synchronizing unit of said working system requests said serial synchronizing unit of said standby system for permission to accept said data; and

said serial synchronizing unit of said standby system, upon receiving said request for permission to accept said data, and moreover, when data from said input device are stored in said input buffer; both sends permission to accept said data to

said serial synchronizing unit of said working system and causes said serial data input/output unit to execute processing of accepting said data.

5. The information processor according to claim 2, wherein said service processor, upon receiving notification of the occurrence of a fault in either of said chip sets, halts the processing in said serial synchronizing unit for synchronizing the operations of said two serial controllers.

6. The information processor according to claim 3, wherein said service processor, upon receiving notification of the occurrence of a fault in either of said chip sets, halts the processing in said serial synchronizing unit for synchronizing the operations of said two serial controllers.

7. The information processor according to claim 4, wherein said service processor, upon receiving notification of the occurrence of a fault in either of said chip sets, halts the processing in said serial synchronizing unit for synchronizing the operations of said two serial controllers.